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| EXAMINER | |
|---|---|
| MULCARE, SHWETA PRASAD | |
| **ART UNIT** | **PAPER NUMBER** |
| 2893 | |

| NOTIFICATION DATE | DELIVERY MODE |
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| 04/16/2009 | ELECTRONIC |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

EFIPLAW@US.IBM.COM

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/596,168 | DOKUMACI ET AL. | |
| | Examiner | Art Unit | |
| | SHWETA MULCARE | 2893 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *10 September 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 June 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *09/10/2008*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Objections*

Claims 6 and 9 are objected to because of the following informalities:

**Regarding claim 6,** change "then" to –than--. Appropriate correction is required.

**Regarding claim 9,** change "an silicon-on-insulator" to –a silicon-on-insulator--

### *Claim Rejections - 35 USC § 112*

**Claims 1-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.**

**Regarding claim 1,** The term "substantially amorphized" in claim 1 is a relative term which renders the claim indefinite. The term "substantially amorphized" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. For purposes of examination, said single crystalline substrate is prevented from becoming "substantially amorphized" when a dopant species is implanted in the sacrificial layer at a dosage that does not damage the crystal structure of the semiconductor substrate.

**Regarding claim 5,** the phrase "using said sacrificial layer" is indefinite. It is unclear in what manner said sacrificial layer is to be used. (Attempts to claim a process without setting forth any steps involved in the process generally raises an issue of

indefiniteness under 35 U.S.C. 112, second paragraph: See MPEP:2173.05 (q) ) Also note that a layer cannot form an implant. An implant can be formed in a layer.

**Regarding claims 6 and 15,** the claim recites "wherein annealing for said halo implant is implemented at a greater temperature and for a longer duration than for said extension implant." However, no annealing step for said extension implant is previously claimed. For purposes of examination, any annealing for halo implant will be held to read over the claim.

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

**Claims 1 and 2 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al. (US 6,620,668; hereinafter Lee).**

**Regarding claim 1,** *Lee (figures 2-6 and related text)* discloses a method for forming a semiconductor device (title: MOS transistor), the method comprising:

defining a sacrificial layer (diffusion source layer 20) over a silicon substrate (10; col. 3 lines 55-56);

implanting said sacrificial layer with a dopant species (22 and 26; col. 4 lines 42) in a manner that prevents said single crystalline substrate from becoming substantially amorphized (col. 5 lines 1-5; see 112, 2nd rejection above); and

annealing said sacrificial layer so as to drive said dopant species from said sacrificial layer into said single crystalline substrate (col.6, lines 14-21 and 28-31).

Lee does not disclose that the substrate is a single crystalline substrate. However, MOS transistors were well known in the art to be formed of single crystalline substrates. As such, it would have been obvious to one of ordinary skill in the art at the time of the claimed invention to form the device of Lee on a single crystalline substrate, motivated by the improved conductive properties of such a substrate.

**Regarding claim 2,** *Lee (figures 2-6 and related text)* discloses wherein said sacrificial layer is a dielectric layer further comprising an oxide layer col. 4 lines 5-6)

**Claims 3-8 and 11-17 rejected under 35 U.S.C. 103(a) as being unpatentable over Lee as applied to claim 1 above, and further in view of Bulucea et al. (US 2002/0074612; hereinafter Bulucea)**

**Regarding claim 11,** *Lee (figures 2-6 and related text)* discloses:

defining said sacrificial layer (20) over a patterned gate stack (18) formed on said single crystalline substrate (col. 3 lines 50-66 and col. 4 lines 1-5) forming an implant (22 and 26; col. 4 lines 42) by said implanting said sacrificial layer and said annealing said sacrificial layer (col.6, lines 14-21 and 28-31).

forming an extension implant (col. 6 lines 14-21 and lines 61-64) by additional implanting of sacrificial layer (col. 4 lines 43-48 and col. 5, lines 58-60)

Lee does not explicitly disclose that the first implant is a halo implant and Lee does not disclose an additional annealing step for the extension implant.

Bulucea (figures 16a-16m and related text) discloses forming a halo implant (184P, 180P, 182P; [0270]) but Bulucea forms the halo implant by a different method, namely by implanting through uncovered portions of the sacrificial layer 210 ([0243]) and annealing said sacrificial layer ([0297]-[0298]) in a single crystalline silicon substrate ([0216]) and forming an extension implant by additional implanting ([0239]) and annealing ([0272]).

In view of such diclosure, it would have been obvious to one of ordinary skill in the art at the time of the claimed invention to have used the method in Lee to form halo implants because halo implants eliminate short channel effects transistors. Further it would have been obvious to use the method of Lee to form said implants because Lee's method prevents dislocations and provides a precise method of controlling doping concentration (Lee: col. 1 , lines 60-65)

Further, it would have been obvious to one of ordinary skill in the art at the time of the claimed invention to have performed the additional annealing specific to extension implanting so that the extension implant is not unnecessarily subjected to the annealing conditions of the halo implant which may be greater than what is required for the extension implant.

**Regarding claims 3 and 4,** *Lee (figures 2-6 and related text)* discloses forming an implant (22, 26:col. 4 lines 34-48) wherein, in addition to said dopant species, said sacrificial layer is further implanted with a damage creating species (29) prior to annealing of said sacrificial layer (col. 5 lines 22) wherein said damage creating species further comprises indium (col. 5 lines 33-37).

The difference between Lee and the claimed invention is that Lee does not explicitly disclose a halo implant. However, semiconductor devices are known in the art to commonly comprise halo implants. For instance, Bulucea (figures 16a-16m and related text) discloses forming a halo implant (184P, 180P, 182P; [0258],[0270]) in a single crystalline silicon substrate ([0216]), albeit by a different method than that of Lee.

As such, it would have been obvious to one of ordinary skill in the art at the time of the claimed invention to have used the method in Lee to form halo implants as disclosed in Bulucea because semiconductors are commonly known to comprise halo implants and Lee's method prevents dislocation from occurring and allows for the doping concentration of impurities to be precisely controlled. (Lee: col. 1 lines 60-64).

**Regarding claim 5,** *Lee (figures 2-6 and related text)* discloses the limitations outlined above further comprising forming an extension implant (col. 6 lines 14-21 and lines 61-64) using said sacrificial layer (col. 6, lines 5-14).

**Regarding claim 6,** Lee as modified by Bulucea discloses the limitations outlined above in the rejection of claim 5 including a halo region and an extension region. Lee discloses a single annealing step (col. 6 lines 14-32) and Bulucea further discloses wherein annealing for said halo implant ([0297]) is implemented at a greater temperature (1000-1100°) and for a longer duration (time includes furnace anneal and RTA anneal [0297]-[0298]) than for said extension implant ([0272]: 540-560°; time includes only furnace anneal).

**Regarding claim 12**, *Lee (figures 2-6 and related text)* discloses wherein said sacrificial layer is a dielectric layer further comprising an oxide layer (col. 4 lines 5-6)

**Regarding claims 13 and 14,** Lee as modified by Bulucea discloses the limitations outlined above including formation of a halo implant and Lee further discloses that in addition to said dopant species, said sacrificial layer is further implanted with a damage creating species (29) prior to annealing of said sacrificial layer (col. 5 lines 22) wherein said damage creating species further comprises indium (col. 5 lines 33-37).

**Regarding 15,** Lee as modified by Bulucea discloses the limitations outlined above and Bulucea further discloses wherein annealing for said halo implant ([0297]) is implemented at a greater temperature (1000-1100°) and for a longer duration (time includes furnace anneal and RTA anneal [0297]-[0298]) than for said extension implant ([0272]: 540-560°; time includes only furnace anneal).

**Regarding claims 7 and 16**, *Lee (figures 2-6 and related text)* discloses wherein said sacrificial layer (20) further comprises an oxide layer (col. 4, lines 5-6) formed over a silicon substrate (col. 3 lines 55-56 and 65-66).

Lee discloses the oxide layer has a thickness of 20-400 nm (200-4000 angstroms. col. 4 lines 1-3), however Lee does not explicitly disclose the layer is formed at a thickness of about 15 to about 100 angstroms.

It is known in the art that forming thinner diffusion layers would facilitate diffusion of dopants..

As such, it would have been obvious to one of ordinary skill in the art at the time of the claimed invention to have formed the oxide layer with a thickness of about 15 to about 100 angstroms so as to facilitate diffusion of dopants from said layer to the underlying semiconductor layer. Furthermore, it has been held that it is not inventive to discover the optimum or workable range of a result-effective variable within given prior art conditions by routine experimentation. (See MPEP 2144.05). Note that the specification contains no disclosure of either the critical nature of the claimed dimensions of any unexpected results arising there from. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicants must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir.1990).

**Regarding claims 8 and 17,** Lee discloses wherein a peak concentration of said dopant species is at about a middle of said oxide layer (col. 5 lines 48-57: impurity

concentration greater at 30 than at 34 or 28 and 30 is "middle" of oxide layer). Lee does not disclose that claimed peak concentration is a result of implantation energy; rather Lee discloses it is a result of implantation angle. However, it is known in the art that implantation energy affects dopant concentration. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the claimed invention to have selected implantation energy so as to locate peak concentration in desired area because implantation energy is an easily controllable variable.

**Regarding claim 20,** *Lee (figures 2-6 and related text)* discloses wherein said dopant species comprises boron (B) (col. 4 lines 34-41).

**Claims 9-10 and 18-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee in view of Bulucea, as applied to claims 1 and 11 above, and further in view of Lee et al. (US 2004/0256647; hereinafter '647)**

Regarding claims 9 and 18, Lee discloses the limitations disclosed outlined in the rejections of claims 1 and 11 but does not disclose wherein said single crystalline substrate further comprises a silicon region of a silicon-on-insulator (SOI) device having a silicon thickness of less than about 100 angstroms.

'647 discloses a finFET device with a halo implant ([0098]) wherein the SOI substrate consists of a single crystal silicon on an underlayer of insulating material ([0039]) and silicon layer thickness is less than 100 angstroms (e.g. 50 angstroms; [0037])

As such, it would have been obvious to one of ordinary skill in the art at the time of the claimed invention to have used the method of Lee to form a semiconductor device with the substrate of '647 because finFET devices afford better control over the depletion region as well as better control of crystal graphic distribution.

**Regarding claims 10 and 19,** , Lee discloses the limitations disclosed outlined in the rejections of claims 1 and 11, but does not disclose wherein said single crystalline substrate further comprises a silicon region of a field effect transistor (FET) device having a thickness of less than about 200 angstroms.

'647 discloses a finFET device with a halo implant ([0098]) wherein the single crystal silicon substrate ([0039]) has a silicon layer thickness of less than about 200 angstroms (50 -150 angstroms; [0037])

As such, it would have been obvious to one of ordinary skill in the art at the time of the claimed invention to have used the method of Lee to form a semiconductor device with the substrate of '647 because finFET devices afford better control over the depletion region as well as better control of crystal graphic distribution.

## *Conclusion*

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SHWETA MULCARE whose telephone number is (571)270-5767. The examiner can normally be reached on Monday to Thursday 7:30 to 5:00 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Davienne Monbleau can be reached on 571-272-1945. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/S. Mulcare. /
Examiner, Art Unit 4183
Thursday, April 2, 2009

/Davienne Monbleau/
Supervisory Patent Examiner, Art Unit 2893